REMARKS

The specification, claims, and drawings were objected to. Claims 1-14 were rejected under 35 USC § 112, first paragraph, as failing to comply with the enablement requirement. Claims 15-17 and 19 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claims 18 and 20 had limitations with insufficient antecedent basis.

Claims 15-20 would be allowable if rewritten to overcome the rejection under 35 USC § 112, second paragraph, as being indefinite.

The indefinite term "N" is being defined as a whole number in amended claim 15. Thus claim 15 should now be definite and overcome the rejection under 35 USC § 112, second paragraph.

Claim 18 improperly referred to a first and second snoop tag partition by not including the word "means". The word means is being added to claim 18, line 11. However, claim 18, lines 31, 33 does include the word "means", so lines 31, 33 properly refer to the antecedents "first snoop tag partition means" and "second snoop tag partition means" at lines 4, 8 of claim 18. Thus claim 18 should now have proper antecedent basis. Applicant therefore requests that claim 15-20 be allowed.

Drawing Objections

The drawings were objected to under 37 USC § 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the feature of "a plurality of local processors for executing instructions and reading and writing data; and a plurality of local caches, coupled to the plurality of processors" recited in claim 2; the features of "a first local cache, coupled between the first processor and the snoop interconnect, for storing cache entries that each store a cache tag and data; and a second local cache,

coupled between the second processor and the snoop interconnect, for storing cache entries that each store a cache tag and data" must be shown or the features canceled from the claims.

Applicant's Figure 4 shows:

a plurality of local processors (70, 72, 73) for executing instructions and reading and writing data;

a plurality of local caches (61, 62, 63), coupled to the plurality of processors (70, 72, 73);

a first local cache (61), coupled between the first processor (70) and the snoop interconnect (60), for storing cache entries that each store a cache tag and data ("TAG", "DATA" in 61);

a second local cache (62), coupled between the second processor (72) and the snoop interconnect (60), for storing cache entries that each store a cache tag and data, ("TAG", "DATA" in 62).

Thus Applicant submits that the drawings as filed show these features of the claimed invention. Applicant requests that the drawing objections be withdrawn.

35 USC § 112, First Paragraph Rejections

Claims 1-14 were rejected under 35 USC § 112, first paragraph, as failing to comply with the enablement requirement. In particular, the limitation from claim 1 "wherein the cache-index portion further comprises a snoop-index portion having the snoop index for selecting the selected snoop set, a chip-select portion, and an interleave portion;" is not enabled by applicant's disclosure. Applicant respectfully disagrees.

Applicant's Figure 6 shows a cache address "L2_ADR" above and a snoop address "SN_ADR" below. The middle portion of the cache address, between the tag and offset, labeled "L2_INDX" teaches the "cache-index portion" of claim 1.

The vertical dashed lines show that this cache index portion "L2_INDX" is composed of a snoop-index portion "SN_INDX", a chip-select portion, "CHIP#", and an interleave portion "SEL".

Applicant's specification at paragraphs 44-46 describe this part of Figure 6:

[Para 44] The middle 13 bits, A17:A5, are the index into the local cache. This index selects one of 8,192 rows or sets in the local cache making or receiving the data or coherency operation request. Each row in the local cache has four entries for a 4-way set-associative cache, and each entry has a tag that must be compared, data, and valid, dirty, and perhaps other cache-management bits such as least-recently-used (LRU) bits.

[Para 45] The middle 13 bits, A17:A5, are further divided for the snoop address. The lowest cache-index bit, A5, is the interleave bit that selects one of the two snoop tag partitions on a chip. Chip-select bits A9:A6 select one of 16 chips in a system. When the system has fewer than 16 chips, fewer chip-select bits are needed and the unneeded chip-select bits are added to the snoop index.

[Para 46] Upper index bits A17:A10 are the snoop index bits. These 8 bits select one of 256 rows or sets of snoop tags within the selected snoop tag partition. Each set of snoop tags can have multiple snoop entries, each with a different snoop tag, since the snoop tag partitions are set-associative.

A person with skill in the art will be able to make and use the claimed invention after reading these paragraphs and looking at Applicant's Figure 6. Applicant thus submits that the enablement requirement has been met. Applicant requests that the rejection of claims 1-14 under 35 USC § 112, first paragraph, be withdrawn.

Claim 5 was rejected under 35 USC § 112, first paragraph, as failing to comply with the written description requirement. In particular, the specification fails to describe how in expanding the multi-processor system, the number of address bits in the snoop-index portion of the snoop address could be decreased to increase the number of address bits in the chip-select portion. Applicant respectfully disagrees.

Paragraph [Para 45], cited above in its entirety, states how bits may be traded off as the system size is reduced:

When the system has fewer than 16 chips, fewer chip-select bits are needed and the unneeded chip-select bits are added to the snoop index.

This sentence teaches that as the system size decreases (fewer than 16 chips), fewer chip-select bits are needed, since there are fewer chips to select from. The unneeded chip-select bits are added (or transferred to) to the snoop index.

The opposite would be true as the system size is increased:

When the system has ~~fewer~~ more than 16 chips, more~~fewer~~ chip-select bits are needed and the ~~un~~needed chip-select bits are ~~added~~ subtracted ~~to~~from the snoop index.

The revisions above are not part of the original disclosure, but show how a person of skill in the art can easily understand how to adjust bits as the system size in increased rather than decreased.

Thus as the system size increases (more than 16 chips), more chip-select bits are needed, since there are more chips to select from. The extra needed chip-select bits are taken (stolen, or transferred from) from the snoop index.

Applicant's disclosure teaches design trade-offs as the system size changes. Larger systems need more chip-select bits, and these extra bits are taken from the snoop index. Thus the limitation from claim 5 is described in the specification:

> wherein the multi-processor system is expandable by adding additional cluster chips to the multi-processor system and by increasing a number of address bits in the chip-select portion and decreasing a number of address bits in the snoop-index portion of the snoop address.

A person with skill in the art will be able to make such engineering design trade-offs after reading these paragraphs and looking at Applicant's Figure 6. Applicant thus submits that the written description requirement has been met. Applicant requests that the rejection of claim 5 under 35 USC § 112, first paragraph, be withdrawn.

In view of the above, it is submitted that claims 1-20, as amended, are in a position for allowance. This application was filed with formal drawings that have not been amended. Applicant believes that a full and complete response to the office action has been made. Reconsideration and re-examination is respectfully requested. Allowance of the claims at an early date is solicited.

If the Examiner believes that a telephone interview would expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (831) 476-5506.

Respectfully Submitted,

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